HIGH SPEED EMBEDDED DRAM WITH SRAM-LIKE INTERFACE

ABSTRACT OF THE DISCLOSURE

The invention provides a simple interface circuit between a large capacity, high speed DRAM and a single port SRAM cache to achieve fast-cycle memory performance. The interface circuit provides wider bandwidth internal communications than external data transfers. The interface circuit schedules parallel pipeline operations so that one set of data buses can be shared in cycles by several data flows to save chip area and alleviate data congestion. A flexible design is provided that can be used for a range of bandwidths of data transfer and generally any size bandwidth ranging from 32 to 4096 bits wide can use this same approach.